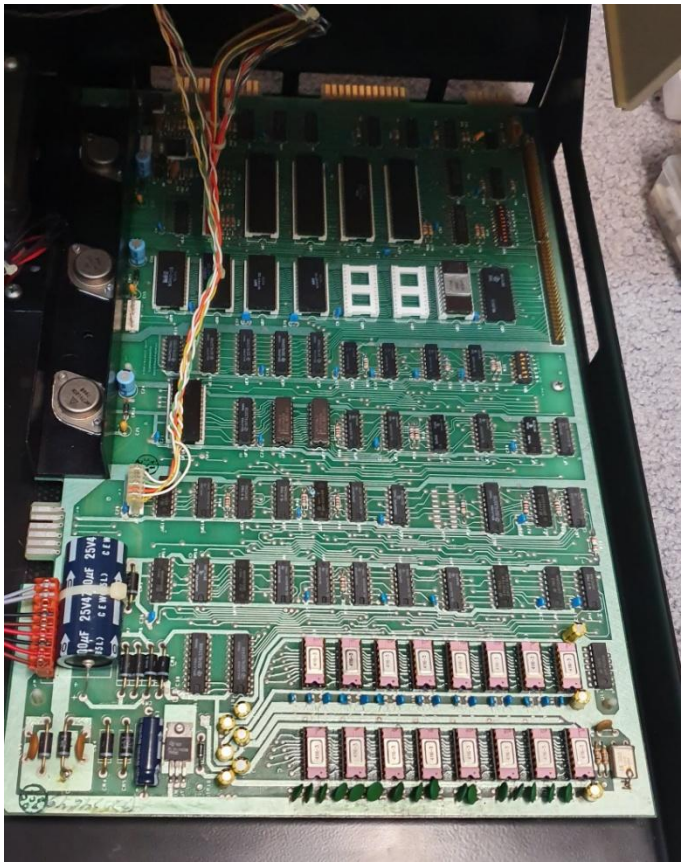
REPAIRING VINTAGE PET COMPUTERS. Part One:

ANALYSIS OF THE PET COMPUTER'S NON - CRTC CHARACTER ADDRESS GENERATOR (CAG)

H. Holden Feb. 2025.



INTRODUCTION:

There are many model variations of PET computers. This article refers to a type of mother board known as "The Dynamic PET" characterized by having 4116 Dynamic Memory IC's and 2114 Static Video RAM IC's. Also it does not contain a CRTC (Cathode Ray Tube Controller IC) Therefore to make sure there are no mix ups, refer to the photos above and the schematics below. It may or may not exactly match your particular PET. This is the only PET I own, so I am not in a position to perform a similar analysis on the other types/models.

The intention of this article is to describe how this PET's Character Address Generator (CAG) system works and also to provide the Operating Theory and Pulse Data on it. The idea is to help Technicians diagnose and repair it, if and when it breaks down.

A detailed Operating Theory is always helpful in making an accurate diagnosis. Better still, a targeted repair on any circuit. The worst approach is random and haphazard guesses, based on hunches and the absence of test data and then unnecessarily removing good vintage IC's from the PCB and risking PCB damage.

THE PULSE COUNTING LOGIC PROBE.

To assist this analysis a Pulse Counting Logic Probe was designed and built. This was simply to check and verify that pulses which were measured with the Tek 2465B, Tek 464 and Hitachi V509 Oscilloscopes were all present and accounted for and that no narrow pulse events, in a pulse stream, had been missed in the analysis.

One reason for this double check is that some of the pulses in this particular circuit are extremely narrow in the region of 100nS to 300nS wide and relatively infrequently occurring. This renders them not easily seen on typical scope recordings. They are either not there frequently enough, or long enough, per cycle, to excite the screen phosphor on a typical Analog scope, or are missed completely by a too low a sample rate on some Digital scopes.

MORE ABOUT THE PET.

The PET computer, it its various forms, has now become quite the collectible item in the World of Vintage Computers. There are a number of reasons why. One is, as the photo above shows, it has a fantastic Retro look to it. And it runs the BASIC operating system which is a relatively easy language for a programming novice, or a Student to learn.

The other reason is that the PET was gifted with a very nice VDU (video display unit) with a CRT. The charm of a real CRT seems somewhat unmatched by a modern flat panel display and inescapably attractive to many, but that might depend if you are a Baby Boomer, Gen X, Y etc.

Most of the PET 9" VDU's had Green CRT phosphors some had White. The PET VDU's did not use composite video signals.

(Composite video signals contain Horizontal and Vertical Sync Pulses. These are used to synchronize independent Horizontal and Vertical scan oscillators in a composite signal input VDU. Therefore the raster scan systems in a composite input type of VDU, much like a typical TV set, can run in the absence the composite signal and its sync pulses)

In many vintage computer systems such as the PET, no raster scan oscillators are present in the VDU and the timing signals from the computer take their place. They are then called Horizontal and Vertical "DRIVE" pulses rather than Sync pulses. This creates the opportunity for malfunction and damage in the VDU, especially if the Horizontal Drive pulses become abnormal in frequency, or duty cycle. This is because the Horizontal scan output stage in the VDU also generates the EHT (extra high tension) voltage and auxiliary voltages for the CRT.

In the 9” Commodore PET VDU, the video signal has no shades of grey. It is simply on or off. The VDU thereby only has a Brightness control. A Contrast control had no application. This is unlike a typical composite video signal VDU. In the typical composite VDU the Analog value of the video component of the composite signal controls the CRT’s beam intensity and the magnitude of those excursions is controlled by a Contrast control. A Contrast control is essentially a video signal amplitude control.

In the Non-CRTC PET discussed here, the H & V DRIVE pulses and the Video pulses are derived from some very creative Logic Circuits using 74 series TTL IC’s.

As new PET models emerged, Commodore, as many did, went to a CRTC chip (Cathode Ray Tube Controller IC). The generation of H & V pulses are done in the one IC. Thereby eliminating the complex array of 74 series TTL based circuits and leaving the one LSI chip to do all the heavy lifting in this department.

Some initial background on the overall PET Character Address Generator (CAG):

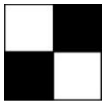
It needs to be understood in the PET that the generation of the H & V DRIVE pulses and the Video pulses are essentially independent of the 6502 CPU.

The way the system was designed is that a video memory “buffer” based on a pair of 2114 1k x 4 bit SRAM memory IC’s holds a byte which specifies the ***address*** of a character to be generated (by a Character ROM). Therefore, to see characters on the VDU at all possible screen address locations, the CAG needs to scan across the addresses of every one of the 1000 screen character locations in the 2114 SRAM.

Regarding the stored byte value at an address in the 2114 SRAM, 7 bits of it are used to specify the Character in the Character ROM.

The POKE command injects a byte value into any specified memory location. In BASIC, if the immediate command POKE 32768,1 is issued, the letter “A” will appear in the first screen character location in the left upper corner of the CRT’s display area.

Or, in another example, if all of the Bits of a byte in a 2114 Video Ram screen location are made logic high, by POKE 32768,255 this graphics symbol appears in the first screen character location in the upper left corner:



And, likewise if the 2114 video RAM was removed from the PCB and its socket outputs held to +5V with pull up resistors, an entire small checkerboard screen will appear because every character address location is seen as having the same binary content (that is if the video circuitry beyond the 2114 and the character address generator is working)

POKE’ing a zero value, or tying the 2114’s output pins low, results in the “@” Character. These tricks can have some applications in troubleshooting the circuitry.

Commodore printed a “translation sheet” (not shown here) which shows what you see on the screen for any decimal value between 0 and 255 POKE’d into any one of the 1000 screen memory locations held in the 2114 SRAM.

There are 1000 screen character locations because there are 40 characters per row and 25 rows, 40 x 25 = 1000, in the particular PET model under discussion.

The 1000 screen locations (from the perspective of the computer user) start at address decimal 32768 and end at 33767.

On the other hand, from the perspective of the electronic 10 bit Character Address Generator (CAG) inside the PET, this circuitry has decimal values from 1 to 1000, represented in Binary form.

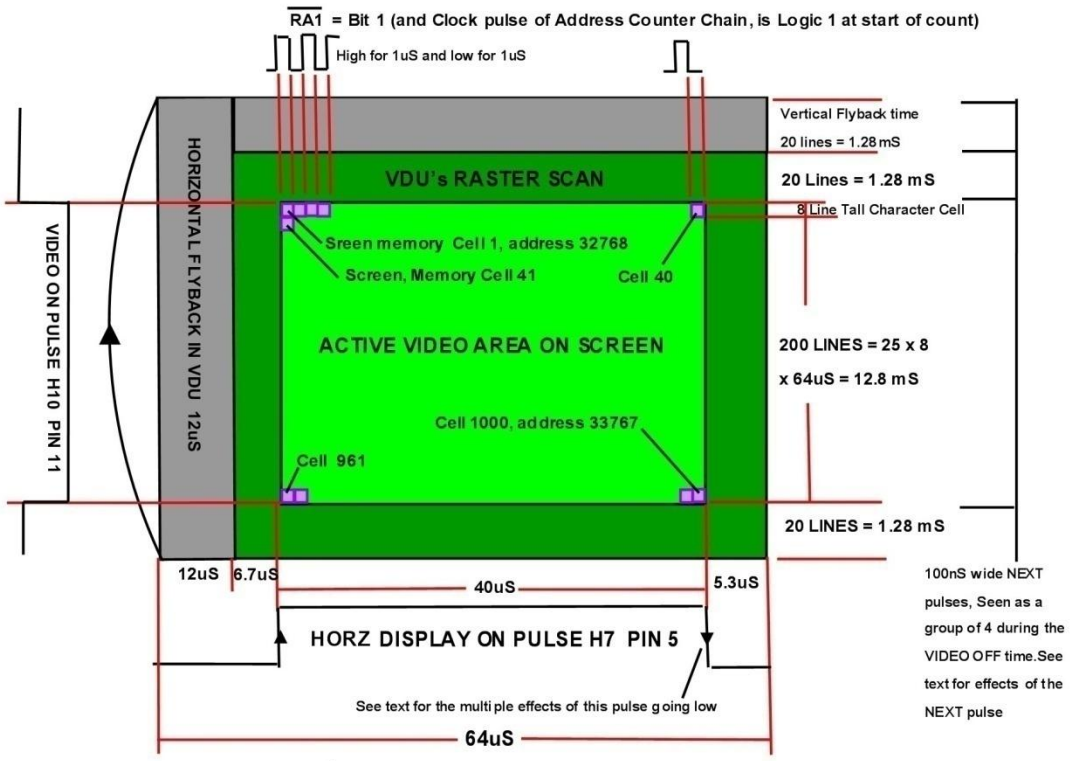
(Some other descriptions of the CAG have focussed on the upper 8 bits of it, controlled by a Latch and a notion of an indexed counting system. However, in this analysis, I have found it better to focus on the whole 10 bits together for a full and detailed description)

It turns out that the lowest address value the CAG can have is 1 and the highest address value 1000 (at the end of active video display time) Or to state that in binary form, considering the 10 bits of the CAG, msb to lsb: 0000 0000 01 to 1111 1010 00. However, the highest count the CAG can get to, in the time frame outside active video display time, when the VIDEO ON pulse is low, is 120 decimal.

The analysis of the CAG might have been super easy, if it were just a counter, free to count as a binary counter does, over some range. However its counting sequences are interrupted, manipulated and controlled by a number of system pulses, such as the HORZ DISP ON pulse, NEXT pulses and /RELOAD pulses. And these will be the issues that are untangled in this article. Untangled, because it is a system of pulse feedback and resets, where the logic conditions of the CAG and some other sub-circuits are detected to create special reset pulses, which after deployment, annihilate the logic conditions that created them, in time frames of 300nS or less.

Getting Started:

To get started, it is better to begin with a diagram of the actual Video Screen and how scanning lines and time are allocated:



Two very important pulses are the HORZ DISP ON pulse and the VIDEO ON pulses. These define the surface area on the video screen where characters are displayed.

The temporal width of a character cell is 1uS as the CRT beam scans the CRT face from left to right. The height of the character cell is 8 horizontal scan lines. The character is made up of 8 pixels horizontally with 8 of those stacked vertically. The illuminated pixels of a character may not fill the whole cell because space is often left beside and below it to space the Number & Letter characters apart. Graphics characters often use the full width of 1uS and the full 8 lines of height.

The total time on the Vertical scan is 3 x 1.28mS + 12.8 mS = 16.64 mS. This makes the frequency of the Vertical Drive pulses to the VDU close to 1/16.64mS or 60.1 Hz. Though, some schematics identify the value at 16.7mS.

The frequency of the Horizontal Drive pulse being 1/64us = 15625 Hz. This represents the 16.0000 MHz Master Crystal Clock Frequency in the PET being divided by 1024.

In the diagram above I have labelled the first character cell, in the upper left hand corner Cell 1 and the last character Cell in the lower right hand corner Cell 1000.

The reason for labelling the address cells 1 to 1000 in this analysis, is that the CAG (the 10 bit binary address counter system) which identifies the addresses of the 1000 screen memory cells, ***when reset to the start of a row of character cells***, always has the Binary value of 1 added to it, it is not zero.

This is because the pulse /RA1, is used as the least significant bit (lsb) of the CAG, and it is the clock for the remainder of the CAG.

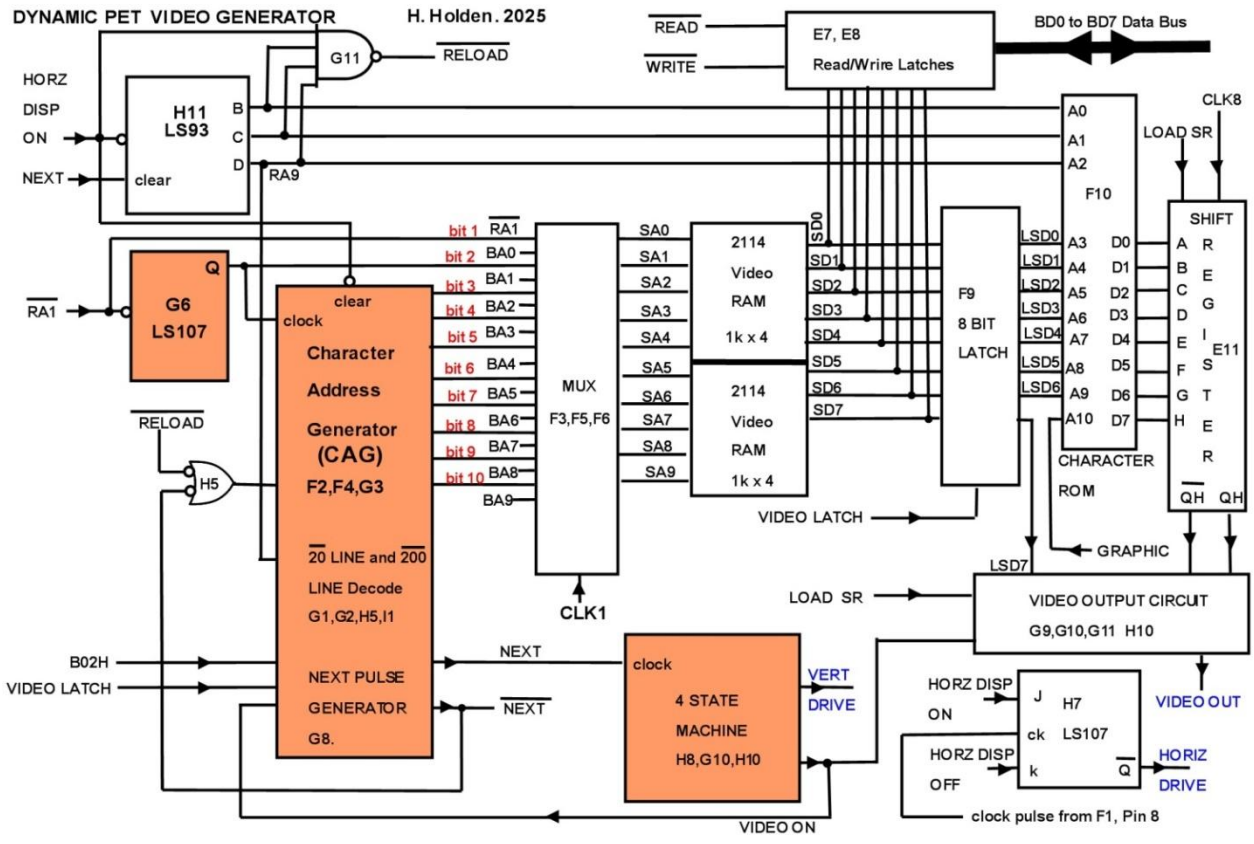
/RA1 has a value of logic 1 at the start of the counting sequence of each of the 40 character cells in a row. Also, when the CAG is reset by NEXT pulses it always returns to a total binary value of 1.

The CAG is only allowed to count, per horizontal scan line, over a time of (40uS) when the HORZ DISP ON pulse is logic high. Otherwise its counting is stalled, because when HORZ DISP ON is low, the flip flop G6 is held in a cleared state and the 74177 counters F2 and F4 are held in a jam LOAD or non-counting condition.

Obviously, if the timing is such that there are 40 characters presented in a row, along a single horizontal scan line, over a time frame of 40uS and each cell is 1uS wide and each cell must have a unique address, then this means the lsb of the CAG counter system, the /RA1 pulse, must be flipping state every one microsecond. Examination with the scope shows that this is the case.

The CAG's labelled outputs, Bit 1 (which is /RA1) to Bit 10 are shown in Red on the diagram below. The CAG, in the diagram below, is shown initially in the orange box as a "block diagram" for now. An initial overview of where the CAG fits in the scheme of things is helpful.

Another "orange box" in the diagram below is the "4 State Machine" which will also be examined later. The diagram below also indicates where the three VDU signals, Vertical Drive, Horizontal Drive and Video to drive the VDU basically originate.



The simplified block diagram above has been created to show how the 10 bits of the CAG sequentially select a specific “cell” or a byte of data at a screen address location in the 2114 video RAM IC’s. The character itself in the Video ROM is clocked out of the Shift Register IC E11 to create the Video signal for the VDU.

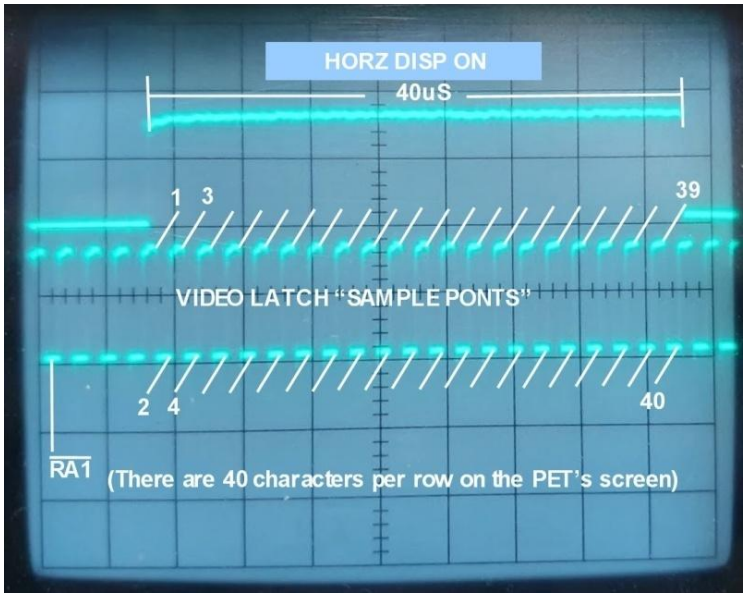
The purpose of the MUX, IC’s F3, F5 and F6 is to allow the CPU to select the addresses of the Video RAM on the other half of the clock cycle of CLK1 and therefore be able to ultimately read or write any byte value from the data bus BD0...BD7 into or out of any one of the 1000 screen character locations via the /READ and /WRITE latches of IC’s E7 and E8.

To display the data represented by memory cells of the 2114 on the VDU’s screen, it is latched by IC F9 and fed to the character ROM as address values. Only 7 bits are latched for the character ROM, because the A10 address input on the Character ROM is used to select GRAPHIC, or the alternate lower case character set that lives in the Character ROM. The 8th bit of data (LSD7) out of the F9 latch is used to invert the data clocked out of out of the shift register E11, so that the characters appear as a black character on an illuminated character cell. Therefore byte values of 128 or over result in the same number or character as those specified by 0 to 127, but they are simply inverted video.

Normally pin 19 (A10) of the character ROM is low, which selects the upper case characters. If you POKE 59468,14 it toggles the pin high and lower case characters are presented. Or if you POKE 59468,12 it goes back to upper case.

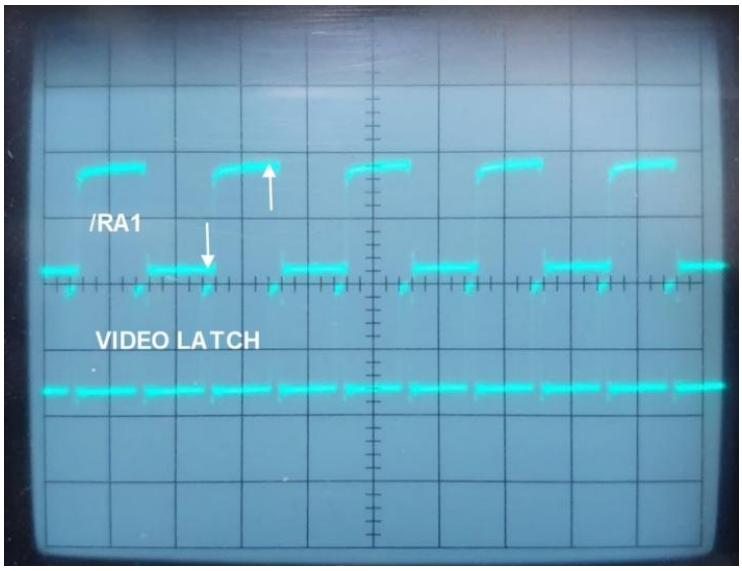
The data latching by F9 is done at a time late in the high part of /RA1 pulse, which as noted forms the least significant bit of the 10 bit CAG. The reason is to make sure that the output data in the 2114 is stable, after it has been presented with the new address of each character cell by the CAG.

The scope recording below shows the timing when the 8 BIT Latch F9, latches (effectively samples) the output data from a memory cell in the 2114’s.



If the pulse counting logic probe tip is connected to /RA1 and if it is gated by HORZ DISP ON, the probe counts a Hex value of 14 (20 decimal) as it is able to count the 20 rising edges of /RA1.

Looking with the scope at /RA1 and the VIDEO LATCH pulses fed to F9 gives a clearer view of that timing:



The NEXT pulses and Digital Circuit Loops:

In essence, the four 100nS wide NEXT pulses are a form of RESET pulse, however they serve another functions too. These pulses are the key to the operation of the entire CAG circuit despite being the more difficult pulses to view with a scope than any of the other pulses in the entire circuit.

The PET's NEXT pulses are derived (extracted and formed) from the pulse streams generated by the /20 LINES and /200 LINES detector circuits. And there are 4 digital reset loops involving the NEXT pulses.

However, the most obvious "circuit loop" people see looking at Commodore's schematic, is the CAG's upper 8 bits (outputs) being fed back to the Latch inputs of G3 and then those latch outputs being fed to the CAG's jam load inputs on IC's F2 and F4. This is just one of the digital circuit loops involved. The other 4 loops involve the NEXT pulses:

These can be seen from looking at where the NEXT pulses are fed, because in each case the feedback results in a change to the digital logic that generated the NEXT pulses.

1) One loop results from /NEXT pulses being fed to the CAG's F2 & F4 clear inputs, this clears the upper 8 bits of the CAG.

2) Another loop where the /NEXT pulses are fed via H5 pin 12 & 11 to the G3 Latch. These make the latch transparent and it acquires (remembers) the zero condition created by the clearing of F2 and F4 by the /NEXT pulse applied to the F2 & F4 counter's clear inputs.

3) There is a loop involving counter H11 and Pulse RA9, the counter's msb. Counter H11 is reset (cleared) by NEXT pulses. RA9 contributes to the pulse stream in the /20 LINES detector and ultimately the NEXT pulse extracted from that pulse stream is a reset pulse, which as NEXT pulses do, not only resets the CAG but also the 3 bit counter H11 that created the RA9 pulse.

4) Another loop involves /20 LINES pulse stream. The /20 LINES pulse stream can only exist in the VIDEO OFF time, which is the compliment of the VIDEO ON time, which is created by NEXT pulses controlling the 4 State machine. The first NEXT pulse is generated by the/200 LINES detector and this also controls the state machine to create the VIDEO ON pulse.

In a brief summary:

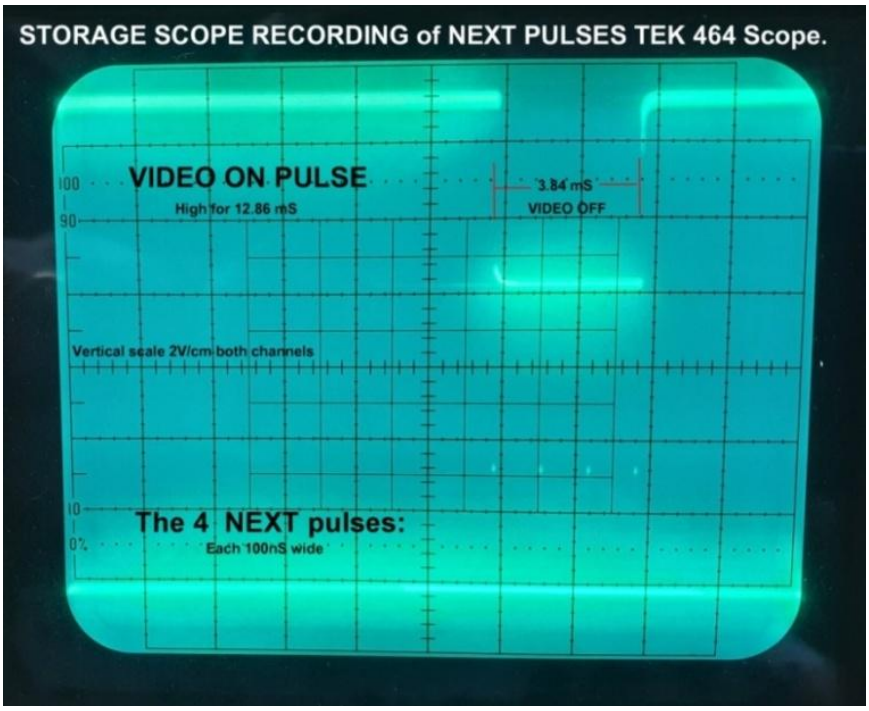
The Latch G3 and CAG logic states are modified by pulse feedback by NEXT pulses and these modify the production of all pulses derived from the CAG, including the NEXT pulses themselves. It sounds like a tautology or some sort of Chicken & Egg problem.

However, we are used to this notion in more simple ways. For example, in a digital counter chain, where some count value is detected by gating. That count can then be used to reset the counter chain that generated it. Then the reset pulse itself becomes "self-terminated" by the feedback process, because the logic condition in the counter chain which created the reset pulse has now vanished. In these sorts of circuit configurations, reset pulses that ultimately terminate themselves are often very narrow and only exist for time frames related to the total propagation time of gates and flip flops, counters etc in the circuit loop involved.

This concept is basically the case for the four NEXT pulses in the PET, except that in this more complex design, the NEXT pulses are extracted from pulse streams by additional gating to remove unwanted pulses in the stream that would trigger a reset. And after that, the NEXT pulses get formed by flip flop control into four uniform 100nS width pulses.

This arrangement introduces a small delay between the leading edge of the gated pulses (which could be called precursors to NEXT pulses) and the leading edge of the NEXT pulses themselves. The result being that the logic state detected by the /200 LINES and /20 LINES detector circuits, in the region where the precursors of NEXT pulses are detected, is allowed to persist a little longer than they otherwise would if they were used the reset the CAG directly. And the method also causes the production of the NEXT pulses to become synchronous with the rising edge of the VIDEO LATCH pulse. This pulse clocks the flip flop that issues the four NEXT pulses. Perhaps in the way that Yogi Bear was smarter than the average Bear, the NEXT pulses in the PET are smarter than the average RESET pulse.

The NEXT pulses are difficult to see on the scope, because they are only 100nS wide and they come in groups of 4 at a relatively infrequent interval of around 16.64mS. In this case the energy delivered to the screen phosphor on a standard oscilloscope is barely enough to see them. A Storage Scope or high sample rate Digital Scope is better to view them. A recording is shown below. We could number those NEXT pulses from left to right, 1 to 4.

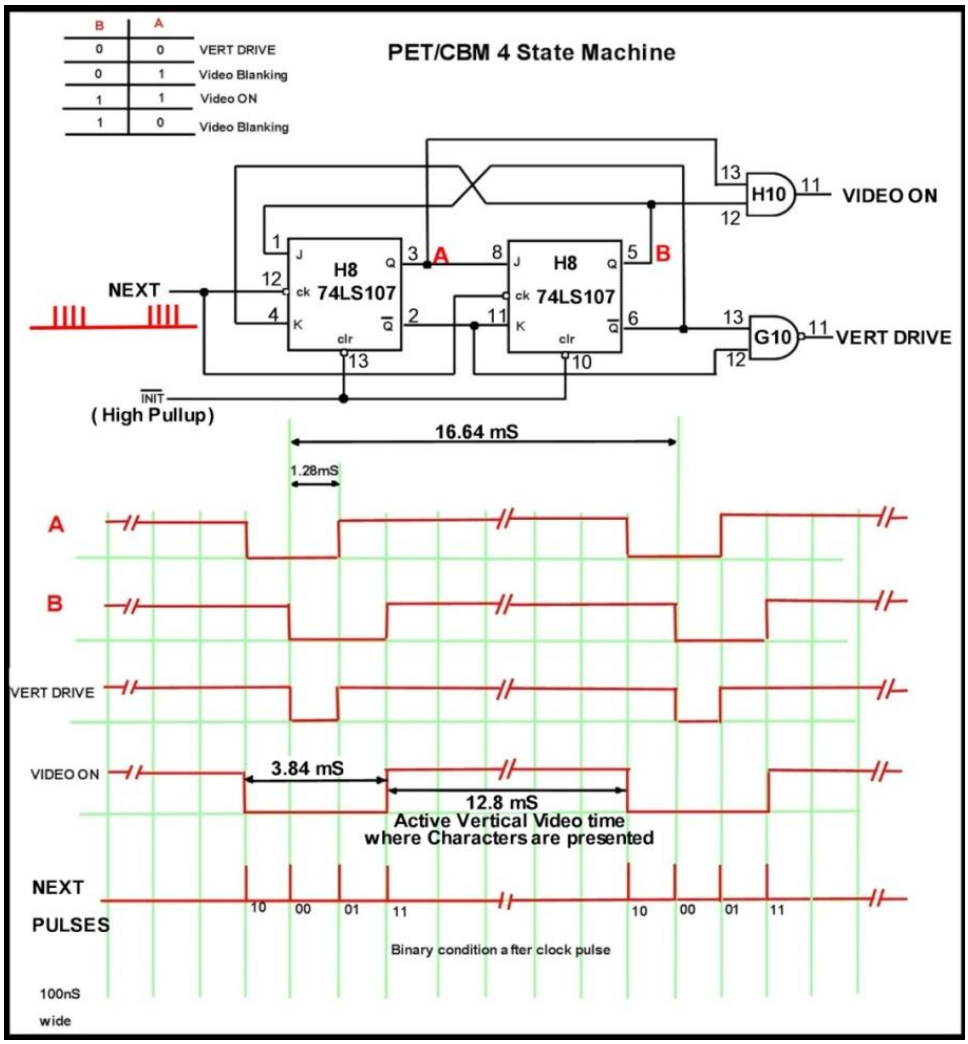


If we are stuck inside a digital circuit loop, where the outputs affect its inputs which again affect the outputs and we want to examine it, where do we start?

Since the four NEXT pulses clock the 4 State Machine it will be examined first because, specifically, the VIDEO ON pulse produced is very important for the production of NEXT pulses.

The 4 State Machine:

This is a two bit counter with a non-standard binary counting sequence and it is clocked by the four NEXT pulses:



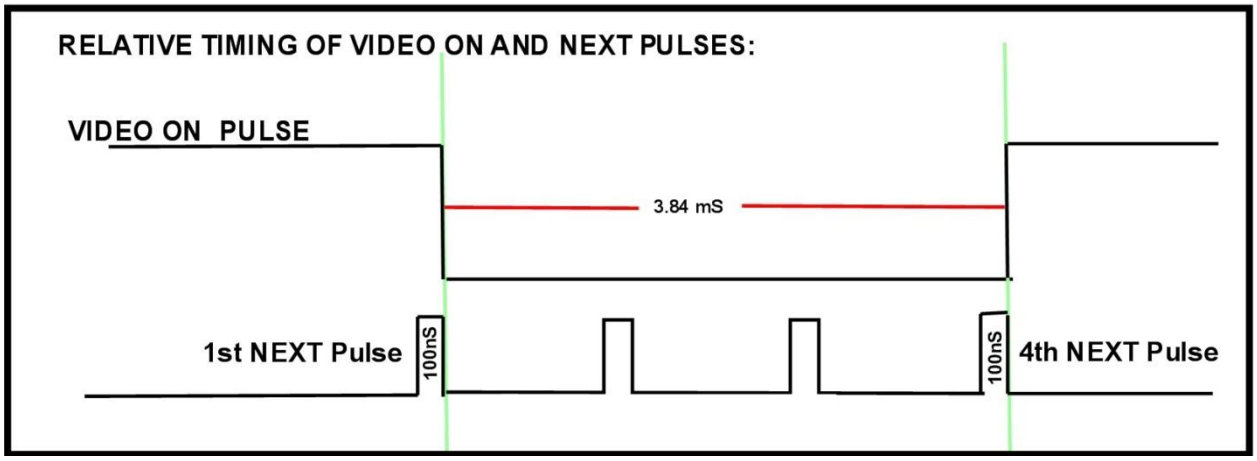
If the Q output if each flip flop is thought of as the msb(B) and lsb(A) of a 2 bit counter, the counting sequence in the State Machine is, 00,01,11,10,00 etc. This is unlike the standard binary counter which counts 00,01,10,11,00 etc. The State Machine generates the VERTICAL DRIVE pulse for the VDU. When this signal is low, it corresponds to the vertical flyback of the CRT's beam which takes 1.28mS.

As can be seen, when the VIDEO ON pulse is low, the four NEXT pulses appear to divide the time into three 20 line or 1.28mS boundaries. And from the 4th NEXT pulse to the first one of the following group of four NEXT pulses, it is 12.8mS or 200 horizontal line periods. These 200 lines are the active video lines where Characters are presented on the VDU's screen during the horizontal time where the pulse HORZ DISP ON is high.

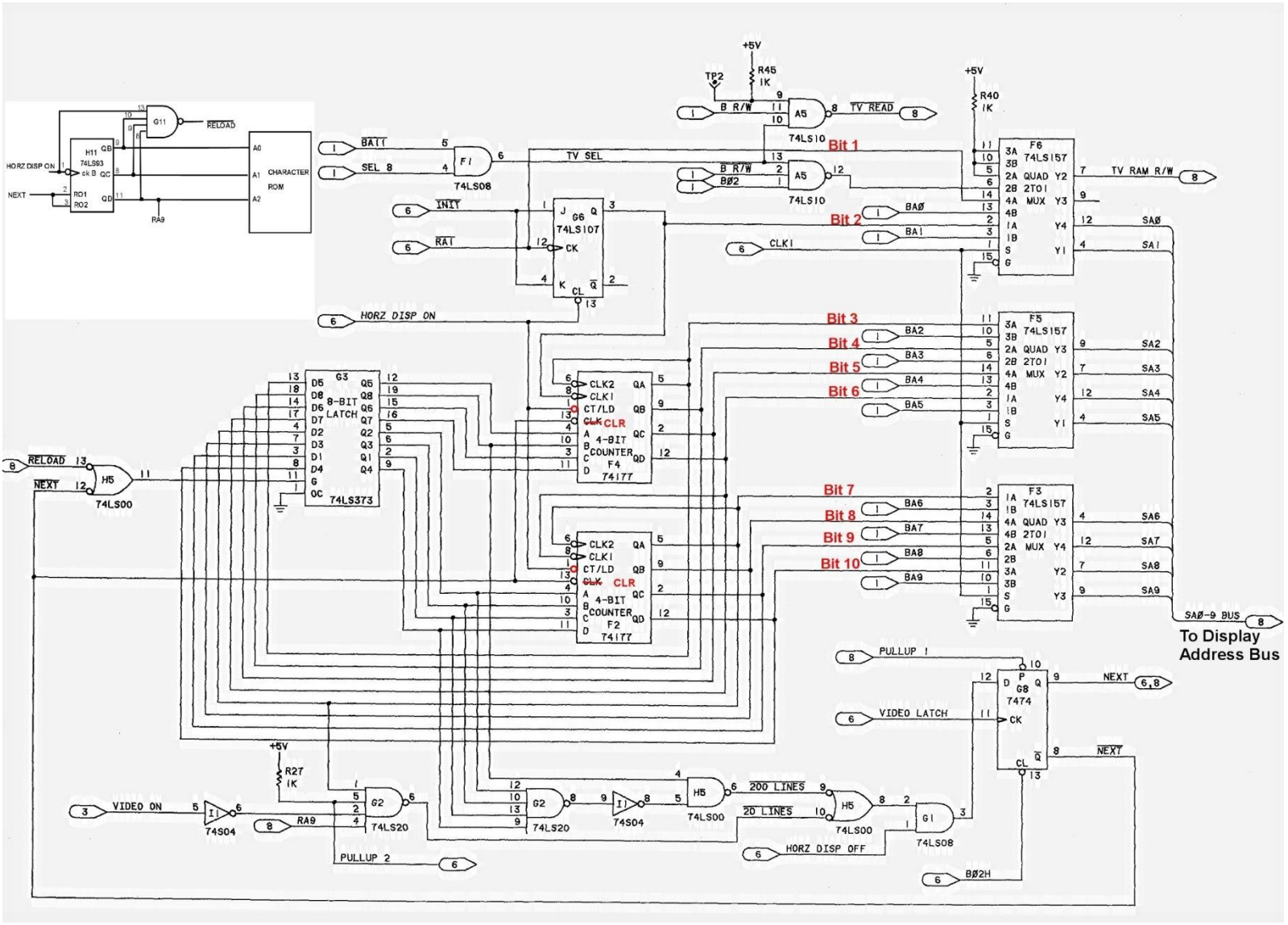
Although it seems unimportant in the scheme of things, because the NEXT pulses are so narrow, compared to the VIDEO ON & OFF timing, it pays to note that the 74LS107 Flip Flops in the 4 State Machine are a Master-Slave type. They change state very shortly after the clock pulse driving them falls *low.*(On the other hand, certain counter chips such as the '161 types used in the pulse counting logic probe shown in this article, are clocked on low to high going pulses)

The exaggerated diagram below shows this. The reason this is shown here is that it has implications in pulse counting, where the VIDEO ON pulse might be used as a gating signal for the pulse counting logic probe, or where it might also be used as an Oscilloscope trigger. Therefore it pays to be aware of the exact relationship.

The Pulse counting probe will count three NEXT pulses if gated to count in the VIDEO OFF time (when the VIDEO ON pulse is low). This is because the 1st NEXT pulse rising edge occurs in the trailing end of the VIDEO ON time. If the pulse counting probe is gated to count for the VIDEO ON time instead, with NEXT pulses feeding the probe tip, it will count 1 pulse, corresponding to the first NEXT pulse in the group of four.



THE CAG - in detail:



It is now necessary to move inside the “box” in the block diagram to look at more details in the Character Address Generator (CAG). To clear up a couple of details (no pun intended) the inputs labelled CLK on the Commodore diagram are the clear (CLR) inputs of the 74177 counters and they are active low.

The Jam Load control input on pin 1 are also active low as designated CT/LD, I added a Red circle to remind me they are active low for jam loading data into the counters.

Whenever HORZ DISP ON pulse is low, the counters F2 and F4 are loaded with whatever values are held in the 8 bit Latch G3. Each flip flop within the 74177 is forced to a Preset or Cleared condition (depending if the loaded bit is high or low) and therefore during this “load” time, they cannot count.

The Latch IC, G3, is made Transparent when its input pin 11 is logic high. This means that its outputs simply follow its inputs. It latches (remembers) the current value feeding the latch when pin 11 goes low. Bits 3 to Bits 10 of the CAG loop back to feed the latch inputs.

Starting with what could be called Line 1 at the top left on the screen area of the first character location and the start of the first line of that character:

Immediately prior to the first active video scan line /RA1 is logic 1 and all the other bits of the CAG, bits 2 to bit 10 are low, because when HORZ DISP ON was off (low) this cleared the flip flop G6, making Bit 2 low. Also, Bits 3 to 10 are low at this time because both the 74177 counters, F2 and F4, were cleared by the 4th /NEXT pulse via H5 pin 12 & 11.

In addition at this starting time of the first line of the 200 Line character block, the data in the G3 latch is zero because the 4th /NEXT pulse, via gate H5 pin 12 & 11 made the latch transparent for 100nS "remembering" the zero condition of the cleared F2 and F4 counters at that time.

To summarize, at this point in the sequence of events, at the very start of the first line of the first character cell, in the upper left corner of the video screen we have:

1) The binary value of the CAG is 1, because RA1/ bit 1 is logic high.

2) The value held in the 8 bit latch G3 is low for those bits.

3) The Q output, Bit 2 of the CAG, flip flop G6 pin 3 is low

4) All the outputs of the 74177 counters F2 and F4 are low

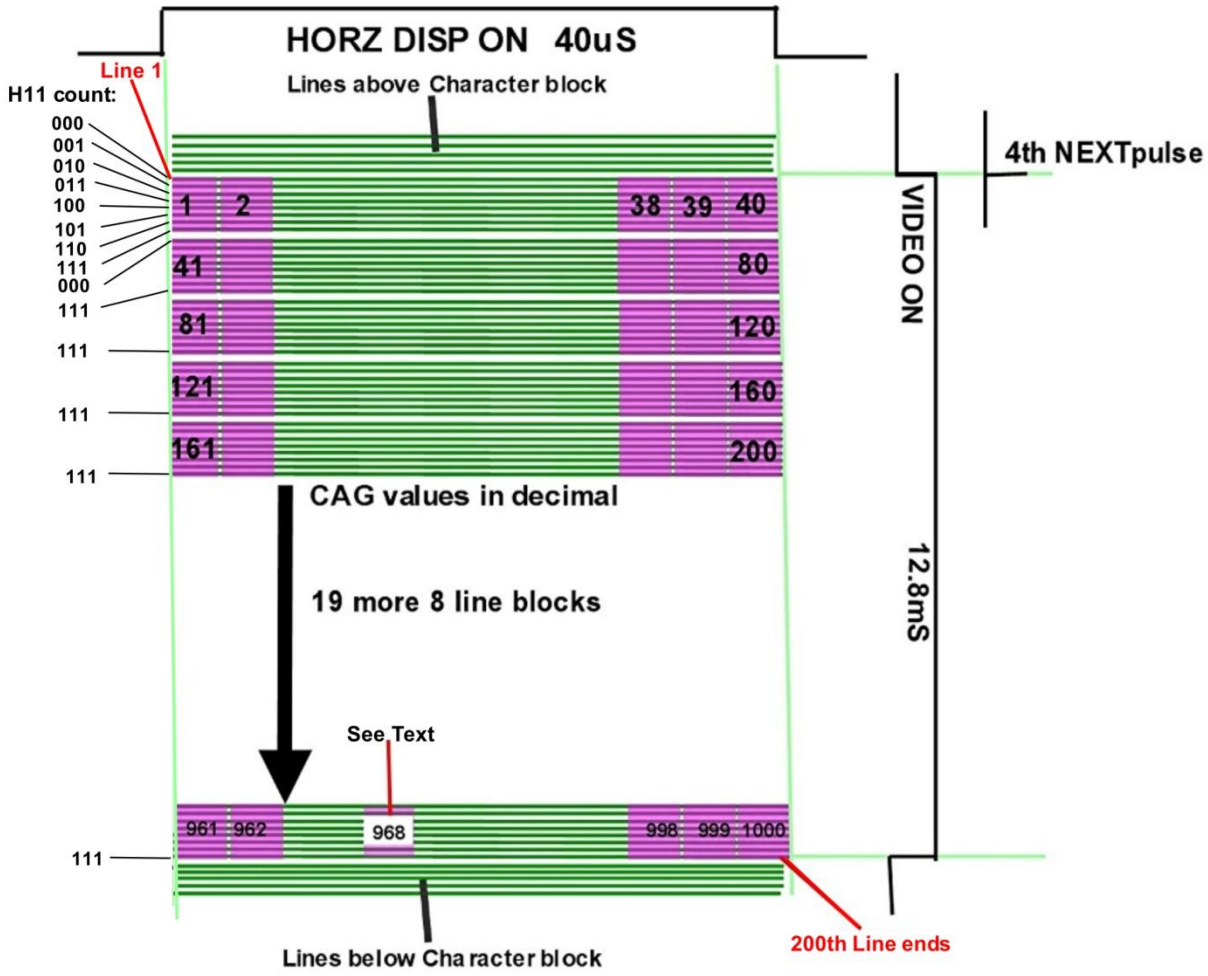
5) The 3 bit binary counter IC H11 (shown added to the upper left of the CAG schematic above) also starts at zero because it was cleared by the NEXT pulse too. This counter is clocked by the HORZ DISPLAY ON pulse, *when it falls low* at the end of active horizontal video time.

G11 decodes the 3 bit count of H11 to create a /RELOAD pulse that deploys on the 8th repeat of the screen address row, for any of the 25 row of characters. When HORZ DISP ON goes high, the CAG then begins counting on /RA1 pulses on going low which change state every 1uS.

The diagram below indicates the counting of the CAG starting at beginning of line 1 which is on the left hand side.

The counting continues along the first line until the total count is 40 decimal. At that point HORZ DISP ON goes low, this clears bit 2 of the CAG and activates the JAM Load inputs on counters F2 and F4 and the counters stop. Since the load value from the latch G3 is all bits zero at this time, the CAG total count (considering the whole 10 bits) returns to 1. The count of the second line is then a duplicate of the first. This occurs until 7 lines in total (most of one character row) have been completed. But, on the 8th line, things change:

The 3 Bit counter H11 is incremented at the end of a line, when HORIZ DISP ON falls low. Therefore at the *start* of the 8th line, the 3 bit counter H11, has a binary value is 111. However to generate a /RELOAD pulse it also requires that the HORZ DISP ON signal is HIGH (due to gate G11) This condition occurs at the start of the 8th line. Therefore, for the whole of the 40uS of the 8th line's active time, the /RELOAD signal is low, thereby making the latch G3 transparent and thereby following the counter's F2 and F4 outputs over that time.

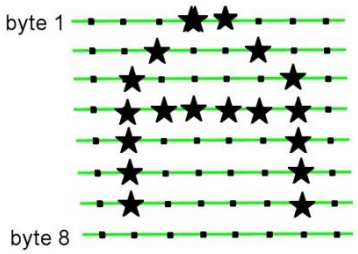


At the end of that 8th line, the HORIZ DISP ON signal goes low, which jams loads the last count value into the counters F2 and F4. The HORZ DISP ON pulse going low clocks the 3 bit counter over to state to 000 after the binary count 111. HORZ DISP ON also terminates the /RELOAD pulse because of gate G11. Fortunately, this does not cause any difficulty because when the Latch G3 is released from reload (from being transparent) it simply remembers the final value it had, which was the value of the upper 8 bits of the CAG, at the end of the 8th line, which was 40 decimal.

When HORZ DISP ON falls low at the end of that 8th line, this takes the Jam load inputs of the counters F2 and F4 low, the counters F2 and F4 are updated (loaded) with the latched value of 40 and hence for the next block of 8 lines, line 9 to line 16, the total CAG count starts at 41.

While the counts along the first 8 lines are being repeated, the output of the 3 bit counter, H11 is keeping track of the 0 to 7 count (8 states) and the three bits are fed into the lsb's of the Character ROM itself. This is because each Character in the ROM is represented there at some starting address, over a range of 8 bytes or 8 consecutive unique addresses. The Character is constructed by individual bytes stacked vertically over 8 scan lines:

If a Dot represents a low bit and a Star represents a high bit in the byte to light up a Pixel, a character, such as an "A" for example is formed in the following manner:



The CAG holds the address of the particular “screen character cell” in Video Memory. The byte content of that cell, 7 bits of it, is used as the address for the upper 7 address lines A3 to A9 of the Character ROM and the lower 3 ROM address lines get scanned along the individual 8 bytes by the 3 bit counter H11, to make up the particular character.

Ultimately the character is presented on the VDU’s screen is applied to a shift register E11 (which serialises it) and is clocked out along the horizontal scan line, to produce the appropriate Pixel pattern, to create that character over 8 consecutive scan lines on the CRT’s face.

The significance of the CAG’s count of 968 in the last character row will be explained shortly.

The /200 LINES and /20 LINES pulses from which the NEXT pulses are derived:

The job of the CAG is not just to generate the addresses to select character cells on the screen. It is vital to the production of the vertical video timing itself. This timing, via the 4 State Machine, generates the VIDEO ON timing and the VIDEO DRIVE pulse for the VDU. The /200 LINES and /20 LINES pulses are a “pulse stream” from which the NEXT pulses are derived.

Although the CAG is only able to count when the HORZ DISP ON pulse is high because it is in a jam loaded condition when it is low, the CAG is free to keep counting during the vertical interval when the VIDEO ON pulse is low (provided HORZ DISP ON is high) in other words in vertical the time window when no characters are being displayed on the CRT.

This time window outside the character display time corresponds to the 20 lines of time (1.28mS) prior to the active video area, the 20 lines of time after the active video area and the 20 lines of time for the Vertical Retrace in the VDU.

During this non-character display part of vertical counting time, which could be called the “VIDEO OFF” time, the same once per 8 line /RELOAD pulse is applied from the 3 Bit counter H11 to the CAG system. It counts in blocks of 8 lines going over the same addresses, just as it does to generate the screen character location addresses in the VIDEO ON time.

/200 LINES pulses:

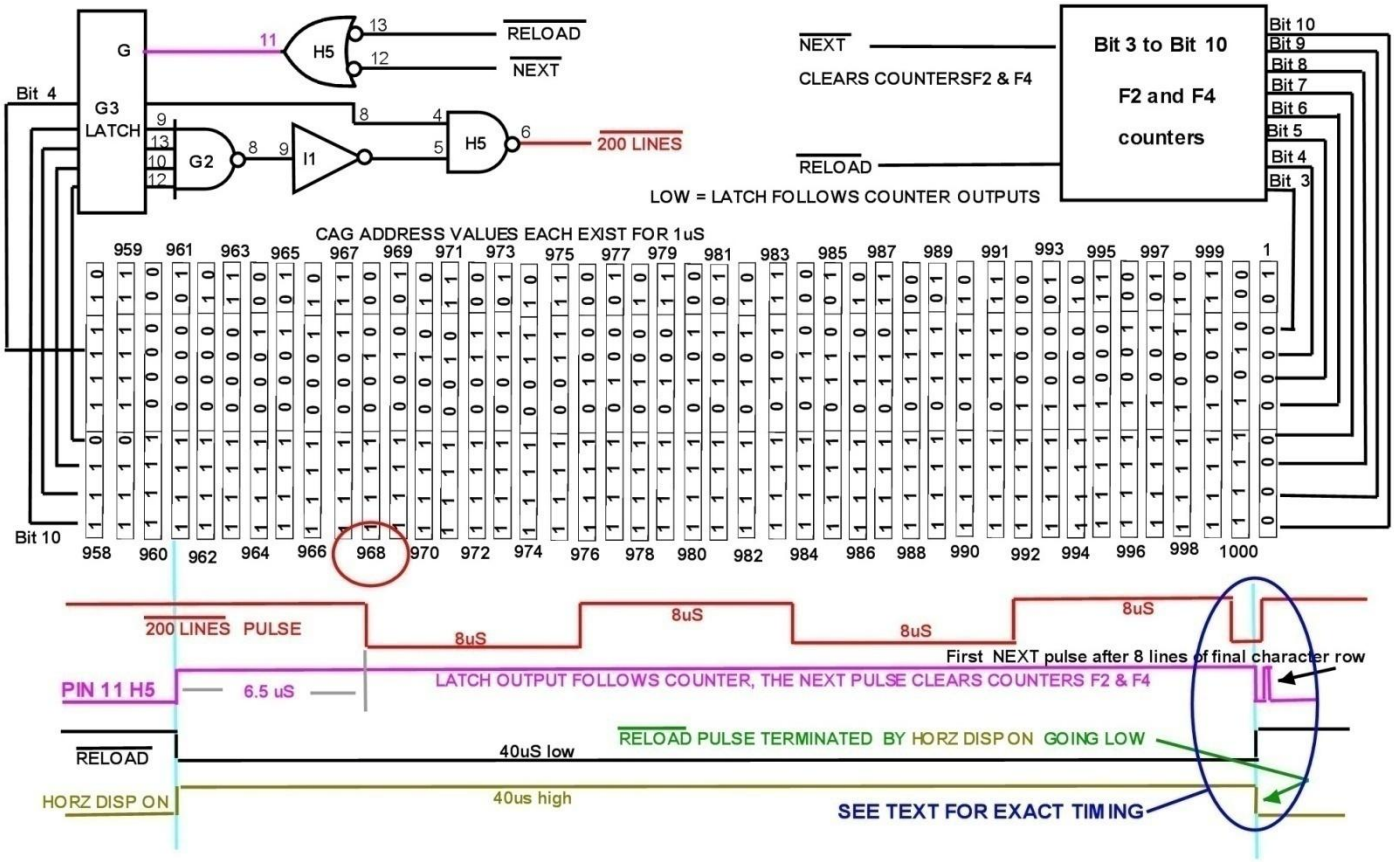
The pulse stream that is the initial /200 LINES pulses are created by gating of five of the latch G3’s output bits. Since the Latch in the first of the 7 lines of the last character block is holding the CAG address at 961 at the start of those lines. No /200 LINES pulses occur. Pulses on H5 pin 6 occur only *on the 8th line of a character block and only on the last row of 40 characters on the 200th line and only when the count has reached 968 or over.* This is specified by the gating by G2, by its input pins 12, 10, 13 & 9 which gate the upper 4 *latched* bits of the CAG and H5 pin 4 being fed by the latched bit 4 of the CAG.

When the G3 latch is made transparent by the /RELOAD pulse, as it is on the 8th line of every 8th line block, the latch outputs correspond to the CAG's upper 8 bits. Bits 7,8,9 and 10 of the latch output are now following the CAG's output are fed to the input of gate G2. The G2 output pin 8 is inverted by gate I1, pins 9 & 8 and NAND gated with Bit 4 by H5, pin 4 & 5 inputs. Therefore to acquire the /200 LINES pulses at pin 6 of H5, all of the five cited CAG's bits must be logic 1. Adding their values up 512 + 256 + 128 + 64 + 8 = 968.

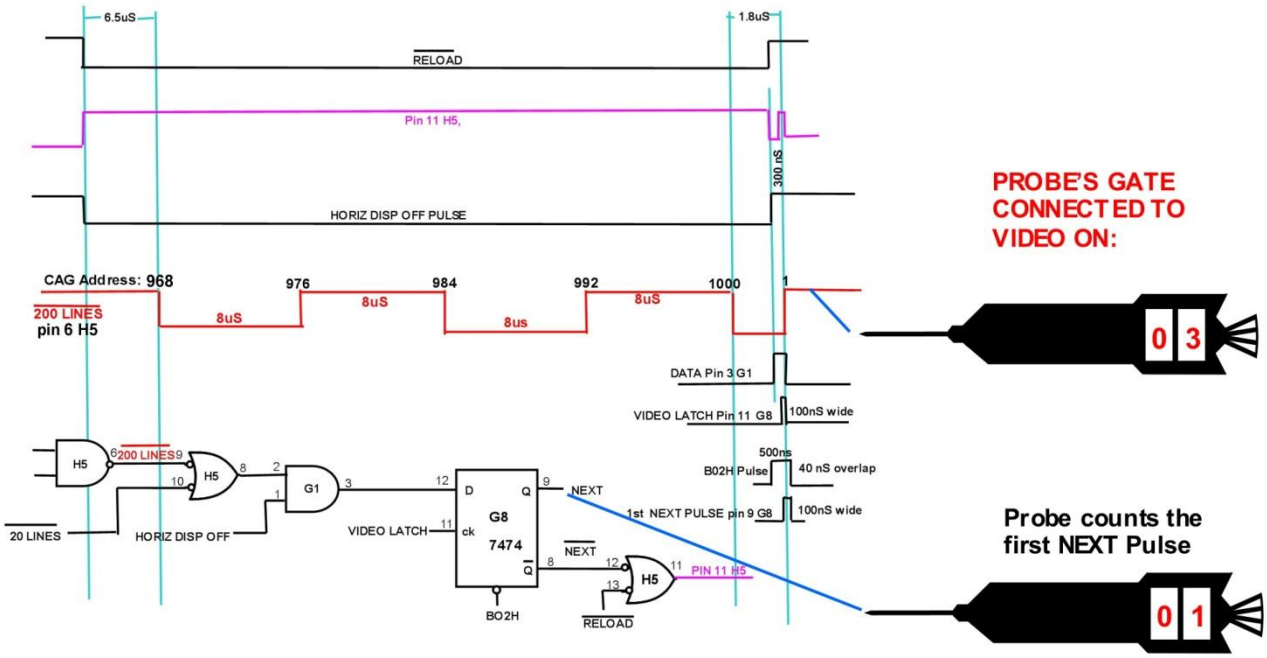
Therefore at the total CAG count of 968, on the last line (200th line) of the bottom row of character cells the /200 LINES pulse H5 pin 6, falls low. Pulses then appear there with a width of 8uS on pin 6 of H5 because of bit 4 of the CAG is going low and high every 8uS while bits 7 to 10 are high. To help make this clear I have created the diagram below which shows the CAG address from count 958 to 1000 and the /200 LINES pulses.

At the end of the 200th line, the CAG does not return to a count of 961, unlike it did in the 7 lines leading to that, because of the first NEXT pulse that is generated by the /200 LINES detector results in a reset of the CAG to binary value 0000 0000 01 and updated the Latch value of zero too.

Notice how Bit 4 is changing logic state every 8uS.



The diagram below shows the timing relationships around the the 1st NEXT pulse in more detail along the 200th line's end and the positive pulse edges counted by the analysis probe. Also for clarity the last 2uS of the trace has been stretched out on the x axis, to make the timing easier to see.



Due to the fact that the 1st NEXT pulse appears in the tail end of the VIDEO ON TIME (remember the relationship of the 1st and 4th NEXT pulse to VIDEO ON) the Logic Probe gated by the VIDEO ON pulse is able to count it. It can also count the three positive going transitions in the /200 LINES pulse stream.

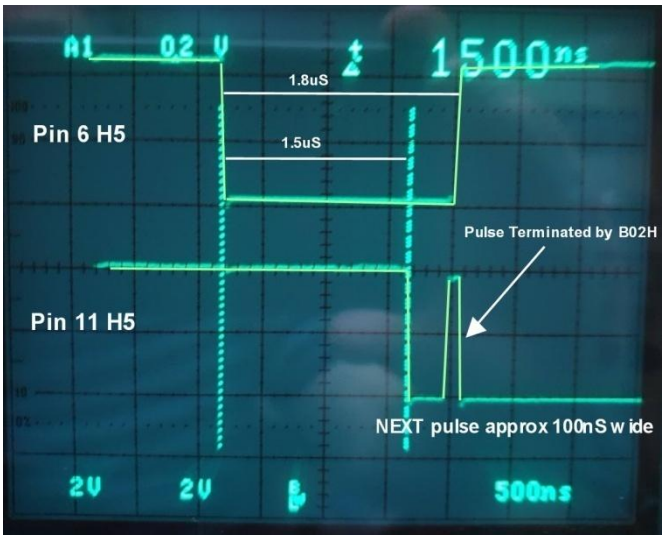
There is a lot happening on the trailing end of the /200 LINES pulse stream, where the first NEXT pulse is generated:

The timing is interesting, in that the NEXT pulse produced is accomplished before the "time is up" for the following CAG address value after 1000, which is reset to an address of 1 by the /NEXT pulse before a 2uS time frame. In other words the address of 1000 in the CAG at the end of the 200th line was allowed to persist for longer than most of the address states, for around 1.84uS (rather than the usual 1uS) but the reset of the CAG to 1 is complete before the end of 2uS corresponding to the next address state for the CAG.

The 8uS pulses that lead to the NEXT pulse precursor are gated out of the Data feeding the Flip Flop G8 pin 12, by the HORZ DISP OFF pulse and the AND gate G1 pins 1,2 &3. This is how the 1st NEXT pulse is derived from the /200 LINES pulse stream and the 8uS pulses eliminated.

Comparing the last low going pulse in the /200 LINES pulse stream on pin 6 H5, with pin 11 H5 which controls the LATCH G3, gives even more timing detail. Using the Tek 2465B Scope's delay B time-base

to see this. Due to the fact the time cursors made the pulse edges difficult to see I drew over them a little in a photo editor:

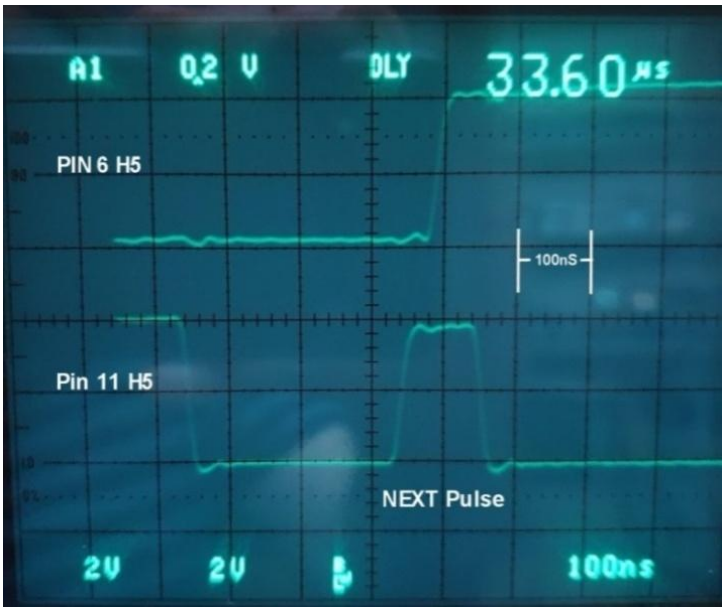


Not only does the /NEXT pulse (inverted by gate H5 pin 12 to 11) allow the latch G3 to become momentarily transparent with the new CAG address value, it also clears both counters F2 and F4, the total address being 1 still because /RA1, the lsb, is high at this time as it is an odd address after the previous even address of 1000.

Looking more closely at another scope recording below, the 100nS wide 1st NEXT pulse; it appears to straddle the rising edge of the last /200 LINES pulse. This is because the flip flop G8 is cleared by pulse B02H which falls low around 40nS afterwards.

The **leading edge** of the 100nS 1st NEXT pulse is created by the leading edge of the VIDEO LATCH pulse which clocks HIGH data to the Q output of the flip flop G8 pin 9. All the above explains how the 1st NEXT pulse is derived from the /200 LINES pulse stream and later formed into this very specific 100nS pulse.

But the most interesting part is that the 1st NEXT pulse going high(at the same time /NEXT goes low, clearing the CAG) is the ultimate cause of pin 6 of H5, the /200 LINES pulse going high again because the logic conditions that caused pin 6 H5 to be low are now eliminated by the reset. It shows a loop propagation delay of something in the order of 50uS after NEXT goes high, or half a NEXT pulse width before the CAG is reset. Possibly explaining why the designers targeted the NEXT pulse to be 100nS because the CAG's new state is likely perfectly stable by the latter half of the 100nS NEXT pulse. Also the end of the NEXT pulse does not extend past what would be the time position for the following address of 1. The address of 1 would persist for around 160nS, before being clocked to 2,3,4 etc with the usual 1uS timing stable on each address.



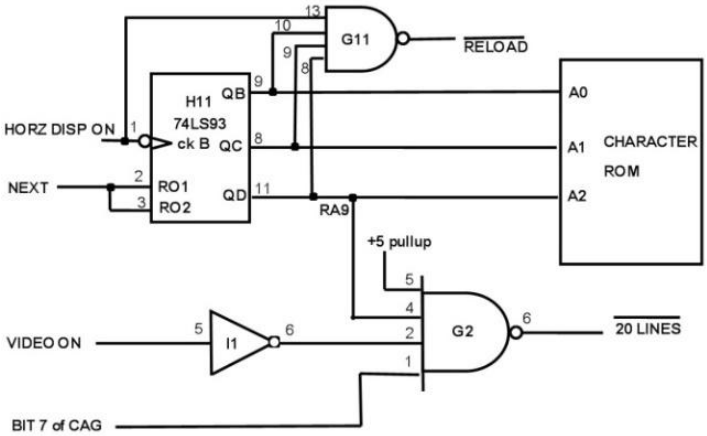
The /20 LINES detector:

Now it is time to explain how the 2nd, 3rd and 4th NEXT pulses are produced by the /20 LINES detector. This is an interesting detector or "encoder" because a unique address did not exist inside the main F2 and F4 counters or the G3 latch system to fully encode it.

This difficulty was because a "20 line boundary" falls inside a zone of repeating CAG addresses. As previously explained, the CAG, regardless of the VIDEO ON or OFF timing, is relentlessly repeating groups of 8 line counts.

Therefore, to "save the day" a pulse RA9 had to be acquired from the 3 bit counter H11 which controls the low ROM addresses and generates the /RELOAD.

The 3 bit counter circuit and reload gate:



The 74LS93 counter H11: The RO1 and RO2 inputs are active high to clear the flip flops within and it was previously noted that the NEXT pulses resets (clears) this 3 bit counter.

For the /20 LINES detector to be operation, the vertical timing is such that it must be *outside* the VIDEO ON time where characters are presented. Therefore the VIDEO ON pulse is inverted by gate I1 pins 5 & 6 to become VIDEO OFF and applied to pin 2 of gate G2.

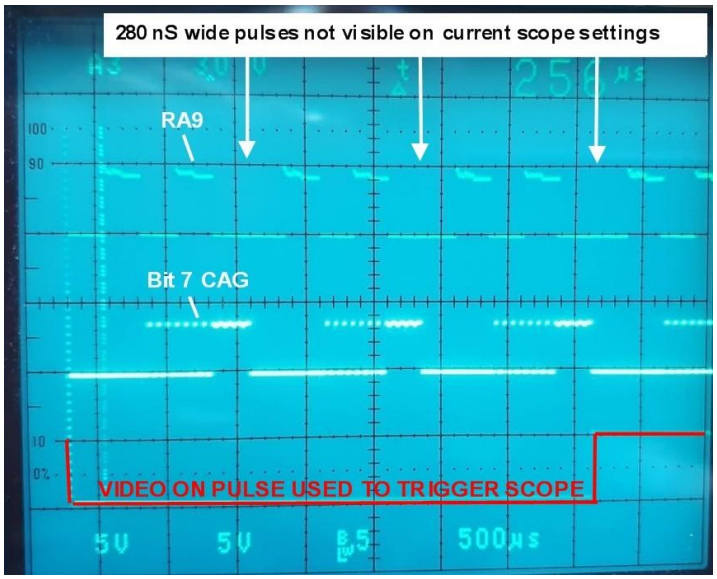
To help understand this circuit (which in many ways is much more tricky than the /200 LINES detector despite having less gates) it is better to examine the scope recordings initially.

For this problem the scope was required to be run in 3 & 4 Channel Mode. One channel is to Sync (trigger) the scope trace to the falling edge of VIDEO ON time in the time block where the 3 remaining precursors of NEXT pulses are generated.

Another channel of the scope is looking the msb of the 3 Bit counter H11 pin 11 (RA9 pulse) and another channel looking at the CAG output Bit 7 because this feeds the /20 LINES gate G2 pin1.

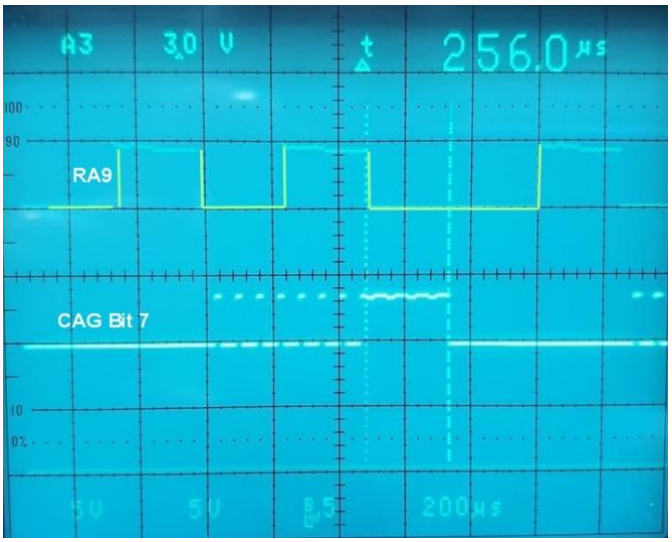
The pulse stream of RA9 appears as a chain of two pulses followed by an apparent missing pulse (though it is actually still there just not easily seen) and this sequence is repeating three times in the VIDEO OFF time when the VIDEO ON pulse is low.

On the other hand Bit 7 of the CAG appears as a chain of seven 17uS wide high going pulses as the count increases with a broad 8th pulse approximately 256uS wide at the end of the 7 pulses. And this pulse array again repeats three times in the VIDEO OFF time window:



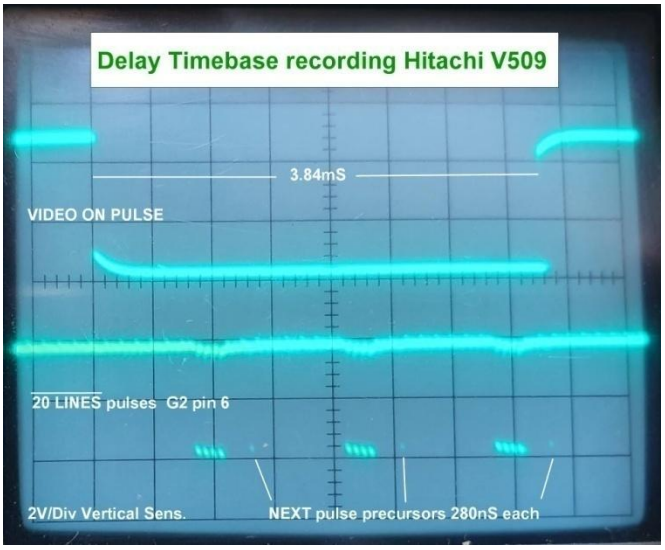
What is not easy to see in the recording above is a very narrow 280uS pulse present in the RA9 pulse stream, in the position noted on the recording with the white arrows. This is the precursor pulse, in each of the three cases, to the 3 remaining NEXT pulses which reset the 3 bit counter that created the RA9 pulse and this results in rapid termination of the RA9 pulse after it goes high.

The recording below shows an expanded view of the relationship between RA9 and Bit 7 of the CAG. Due to the faint traces being difficult to see I have drawn over them in places in a photo editor to make it easier to see:

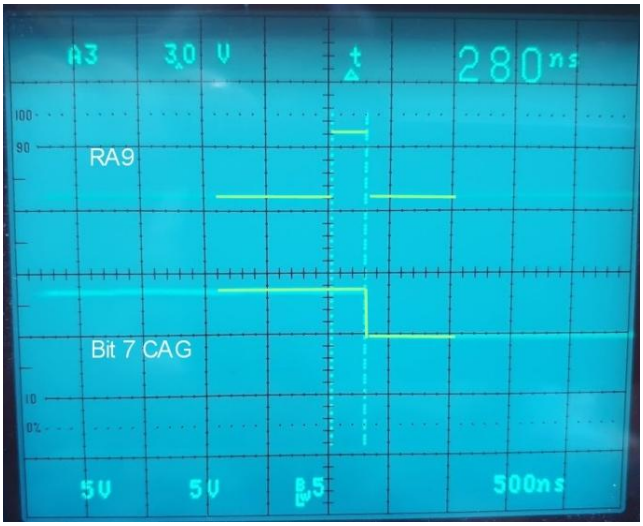


Notice in the recording above, 4 of the initial pulses of the Bit 7 pulse stream, occur at a time when RA9 is low, therefore these 4 pulses do not make it out of pin 6 G2, into the /20 LINES pulse stream.

In addition RA9 falls low again just after the start of the 256uS block of the Bit 7 pulse, this shortens that pulse, so that what remains in the /20 LINES pulse stream, at this point are three groups of 4 pulses, each close to 17uS wide, with a gap leading to the difficult to see 280nS precursor of a NEXT pulse. Therefore, with a typical Scope examination of the /20 LINES pulse, what the observer sees is three groups of 4 pulses with the 280nS ones not easily visible at all. However using the Hitachi V509 scope's on delay time-base I was able to capture the three groups of 4 pulses and just make out the 280nS pulses in the /20 lines pulse stream:



The 2465B scope recording below shows the difficult to see 280nS wide pulse in the RA9 pulse stream (this later becomes a 100nS NEXT pulse) which occurs just before Bit 7 of the CAG falls low:



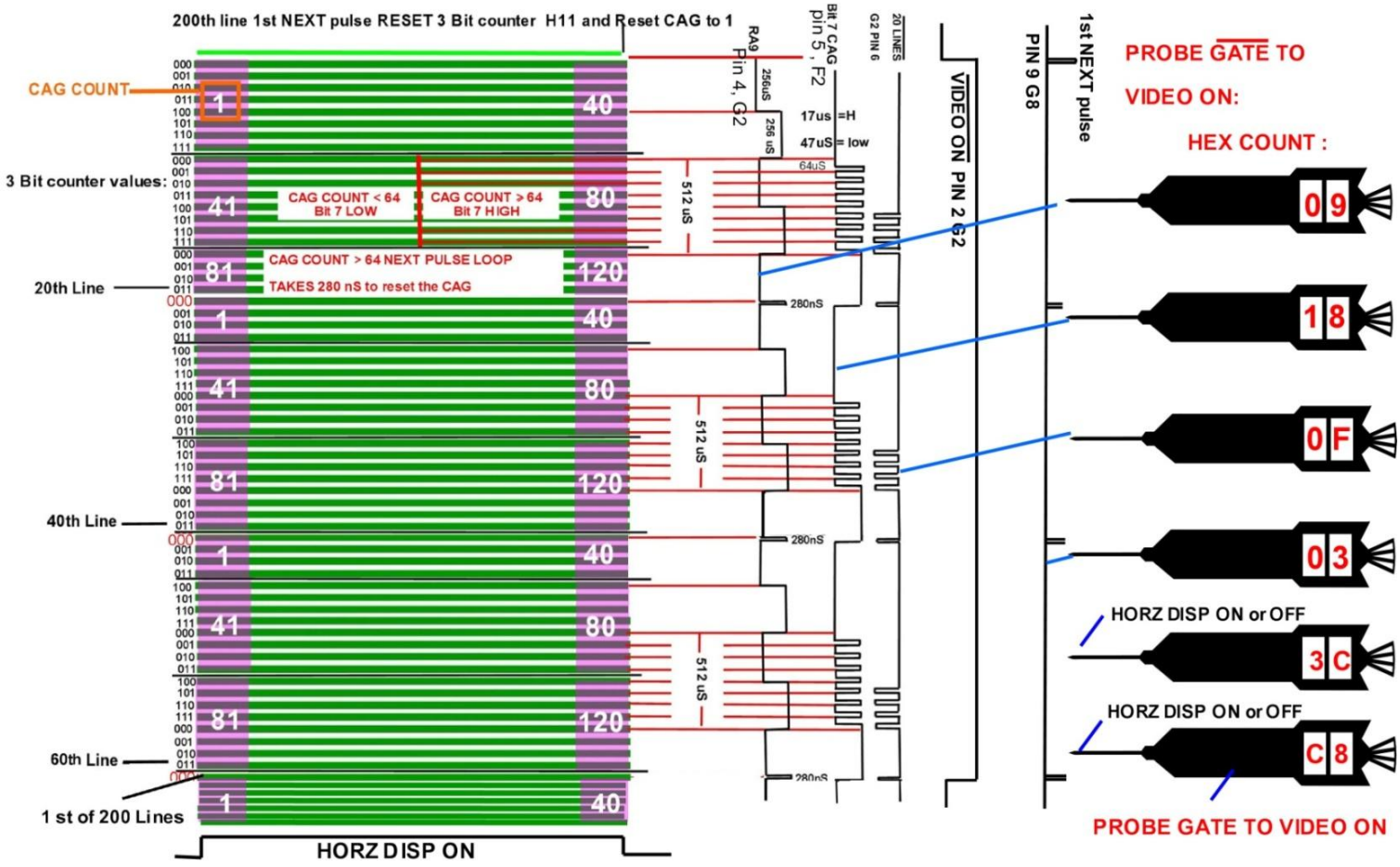
The 280nS “precursor to a NEXT pulse” has its leading edge created by RA9 and it trailing edge terminated by the NEXT pulse it creates, resetting H11 and the CAG and hence both RA9 and Bit 7 fall to logic low.

One final recording below explains how the remaining 4 pulses leading to each 280uS pulse are eliminated by the HORZ DISP OFF pulse and gate G1.

These 4 pulses labelled 1,2,3,4 are gated out by G1 and the HORZ DISP OFF pulse and the only remaining pulse of the /20 LINES pulse stream presented to the flip flop G8 data input, to be crafted into 100nS NEXT pulses, are the three 280nS pulses. (The HORZ DISP OFF pulse also gates out the 8uS pulses of the /200 LINES pulse stream too)

The recording is faint, however when the labelled pulses 1,2,3 & 4 are high, the HORZ DISP OFF pulses are low, thereby eliminating these 4 pulses at the output pf G1 pin 3 feeding the Flip flop G8 that issues NEXT pulses.

To help summarise and re-cap the process of the generation of the three 280nS precursors of NEXT pulses which are generated by the /20 LINES detector, I have placed most of the information on one diagram below, where it is worth going over a few more details again to explain how the /20 LINES pulse stream comes about:



The counting probe values are shown which verify the number of positive going pulse edges with no surprises. In this Video OFF time, the CAG count, due to the resets provided by the NEXT pulses, never exceeds a value of 120 decimal.

If the probe counts in active video time by connecting the probe's GATE input to VIDEO ON on the probe tip connected to HORZ DISP ON (or HORZ DISP OFF), then the count = C8 = 200 as expected.

If the probe's /GATE is connected to VIDEO ON, it is counting in the VIDEO OFF time, then it counts 3C = 60 decimal, or the 60 lines in the block above when the probe tip is connected HORZ DISP ON (or OFF).

The 1st NEXT pulse is not counted by the probe in this Video Off time window because, as previously noted, its rising edge resides inside the VIDEO ON time window.

The pulse RA9 starting at the top where H11 was cleared by the first NEXT pulse from the /200 LINES detector, is the msb (bit 3) of counter H11 going high after a count of 4 lines or 4 x 64uS = 256uS and stays high for another 256uS before the counter rolls over to zero. At the end of the 8th line (when HORZ DISP ON falls low as previously noted) the CAG, taking all bits into account, is loaded with a final value of 41.

Explaining the relative timing of Bit 7 of the CAG vs RA9:

On the 9th line the three bit counter H11 has a value of zero at the beginning of that line because at the end of the 8th line, the low going HORZ DISP ON pulse clocked H11 from a binary state of 111, to 000 and therefore RA9 fell low.

However from the time at the end of the 8th line when RA9 fell low, to the very start of the 9th line in the active video area there is a 24uS delay before HORZ DISP ON goes high again. This is due to the duty cycle of the pulse that is HORZ DISP ON, it is high for 40uS and low for 24us.

After that 24uS delay, the CAG on line 9 has to count from its loaded value 41, to 64, which accounts for another 23uS of clocking time, 24uS + 23uS = 47uS. This is why the rising edge of Bit 7 of the CAG pin 5 of counter F2, occurs 47uS after the falling edge of the RA9 pulse. Also, since to get back to any same Horizontal position on the screen, that cycle time is always 64uS, then the pulses on Bit 7 of the CAG are high for 64uS – 47uS = 17uS as is shown on the diagram.

Anytime the CAG count is greater or equal to 64, Bit 7 is high. As can be seen by the diagram this results in a stream of seven 17uS high pulses on Bit 7 leading to an 8th pulse of 256uS in width as seen on the scope recordings of Bit 7. The pulses are there because in the repeating address range 41 to 80 of the CAG, bit 7 is toggling, but above address 64, in the range 81 to 120 bit 7 is high. It stays high until half way through the third 8 line block, when a NEXT pulse precursor is generated by RA9 going high in a self terminating reset loop by the derived NEXT pulse resetting H11 and the CAG.

To re-cap again the four NEXT pulses have 5 applications at least:

1) Reset and synchronize the 3 Bit counter which controls the lower ROM addresses and the 8 line /RELOAD function to display the characters. Also result in the self termination of pulse RA9 for the /20 LINES pulse stream.

2) The /NEXT pulses clear the upper 8 Bits of the CAG which includes Counters F2 and F4.

3) The /NEXT pulses make the latch transparent G3 and loads the latch with zero because the cleared F2 and F4 counter values are latched.

4) They clock the 4 State Machine. This generates the Vertical scan timing for the VDU and the /VIDEO ON pulse required for gating the 2nd, 3rd & 4th NEXT pulses.

5) They border the 20 and 200 line boundaries and break a 60 line period into 3 parts.

As noted, the NEXT pulses are a developed and elaborate form of RESET pulse, selectively gated out of pulse streams and specifically temporally formed by flip flop control and synchronised by the flip flop to the leading edge of theVIDEO LATCH pulse and they have the effect of ultimately terminating the logic conditions in the CAG counter system which created them in the first place.

Summary:

The PET's Character Address Generator appears to be a Master Class in Glue Logic design using 74 series TTL IC's. Due to its complexity and paucity of information provided by Commodore on how it worked, technicians at times have struggled to repair it. Also the situation is not helped by the very narrow pulses in the circuitry which are difficult to image with the scope. Still, if you know what pulses are supposed to be there and why, then it makes it much easier to look for them and find them, especially with scopes with delay time-base functions or high sample rate digital scopes. Hopefully the description of the CAG above will help in fault finding and repairs.

Generally vintage 74 series TTL chips are fairly reliable, but at times the do fail. Even one logic gate failing in circuitry like this can result in very complex malfunctions. Also TTL chips can have various failure modes. It is usually fairly obvious when their output stage fails and the output voltage goes outside the range of standard TTL logic highs and lows. However, one interesting failure is that sometimes a gate input can go open circuit inside the package. When that happens the chip's die assumes the pin is logic high and a multi-input gate can still produce normal looking output pulses, but they are the wrong pulses.

It is very important to ensure that a gate, Flip-Flop or Counter IC is obeying its logic table, or it can be easy to be caught out by that problem. Certainly a plain pulse detecting logic probe cannot help there.

Other IC's in the PET are not as reliable as the 74 series TTL parts. In many vintage PET repairs the 2114 SRAM IC's have been found to be defective. Also there is a fairly high failure rate of the 4116 DRAM IC's and the PIA and VIA chips occasionally fail. And the GPIB bus driver IC's the MC3446, will occasionally fail. Mostly the 6502 CPU remains reliable.

To help with PET repairs I have created two other highly detailed articles:

REPAIRING VINTAGE PET COMPUTERS. Part Two. DRAM MEMORY TEST SYSTEM FOR THE DYNAMIC PET COMPUTER. This article describes how to diagnose and locate faulty 4116 DRAM IC's so that the faulty parts can be found with having to unsolder good IC's from the PCB. It uses a diagnostic system based on an added hardware module and some custom firmware held in a ROM that is plugged into the board.

REPAIRING THE VINTAGE PET COMPUTER. Part 3. The Dynamic PET's 9 inch VDU. This article describes how to restore and improve the VDU and has a detailed analysis of Flyback Transformers and how to do in-circuit tests and diagnose them and select possible non standard replacements to help repair them because the original parts are very difficult to find now.

****

PULSE COUNTING VERIFICATION LOGIC PROBE TO HELP THE ANALYSIS OF the PET's CAG.

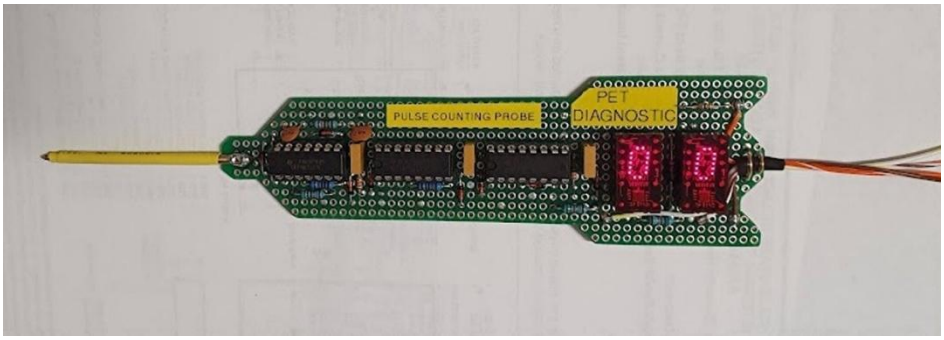
As noted before, this probe was intended as a **verification tool** of the pulse numbers present in a working PET's CAG system, not a service tool. Due to the very narrow pulses, there was a fair chance that I could have missed one with the scope alone and that would have fouled up the analysis of the CAG.

There is no guarantee that in a faulty PET, in the CAG area especially, because of the multiple self terminating pulse feedback loops that correct gate pulses such as VIDEO ON will be present or normal.

Although, the HORZ DISP ON pulse originates outside the CAG loop and the first four bits of the CAG can be checked/counted using HORZ DISP ON as the GATE pulse; bit 1 = /RA1 Hex display 14, Bit 2 pin 3 G6 Hex display 0A, bit 3 pin 5 F4 Hex display 05, and bit 4 pin 9 F4 Hex display 03.

The probe can also be used elsewhere in the PET's circuitry too, provided it is verified that the pulses, used as GATE pulses, are present and accounted for & normal.

The prototype was simply made on plated through hole spot board and hand wired. A pcb foil design has also been made. TIL311 Hex displays are readily available on ebay, expensive from the USA, however they are in the range of $7 to $20 each from China. Another option are the Hex displays made by Avago/Broadcom, however these have a different footprint and the pcb foil pattern would need changing and last time I looked they were no cheaper.



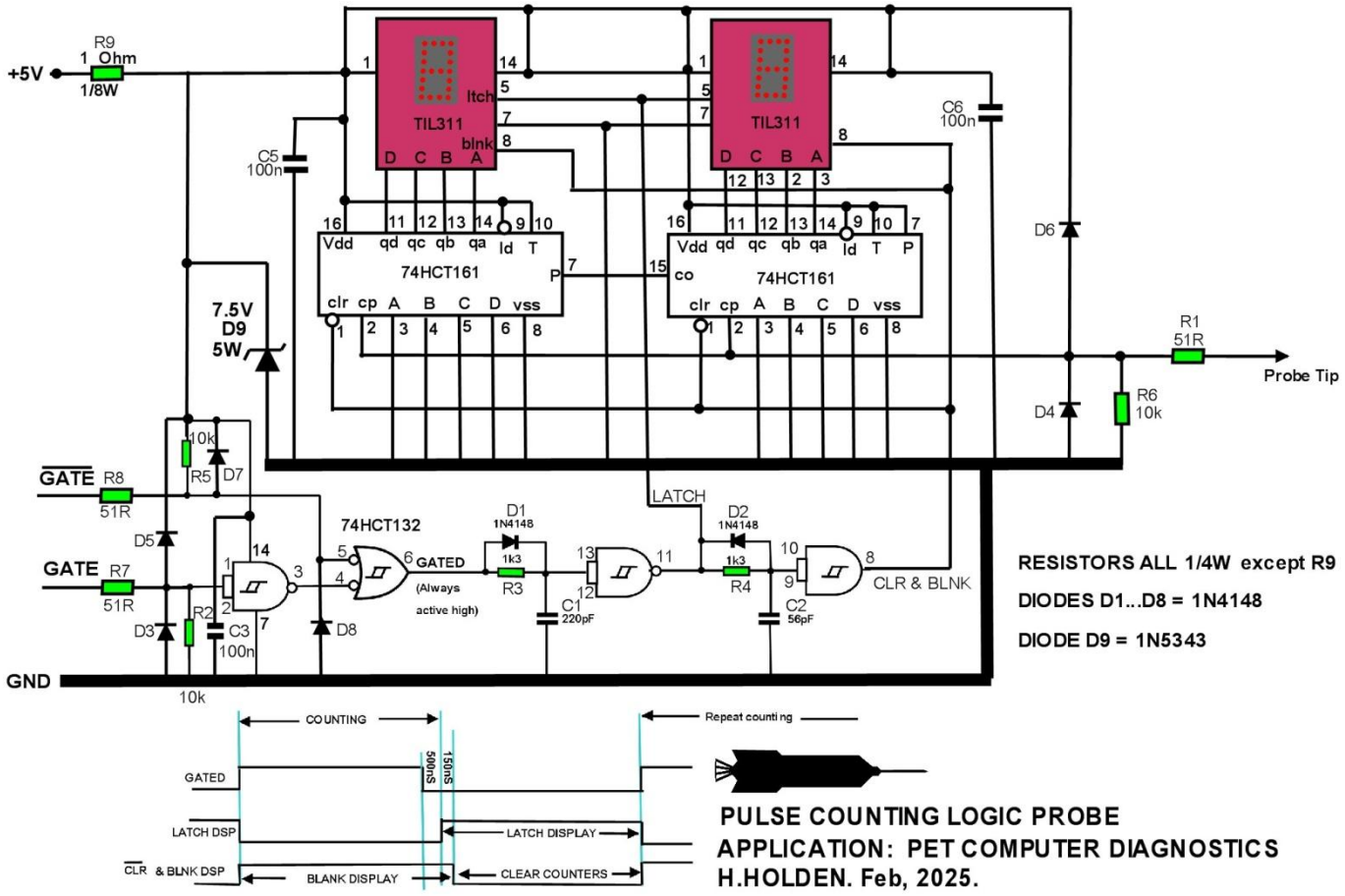
The probe simply consists of two binary counters (74HCT161) which are clocked by the pulse chains in the system at specific test point. The counting is gated into operation typically by either the HORZ DISP ON pulse or the VIDEO ON pulse in the PET application used here, but the probe can also be gated by many other signals and be used in other systems.

When the PET's circuitry is functioning normally a specific number of pulses appear in specific time windows throughout the circuitry.

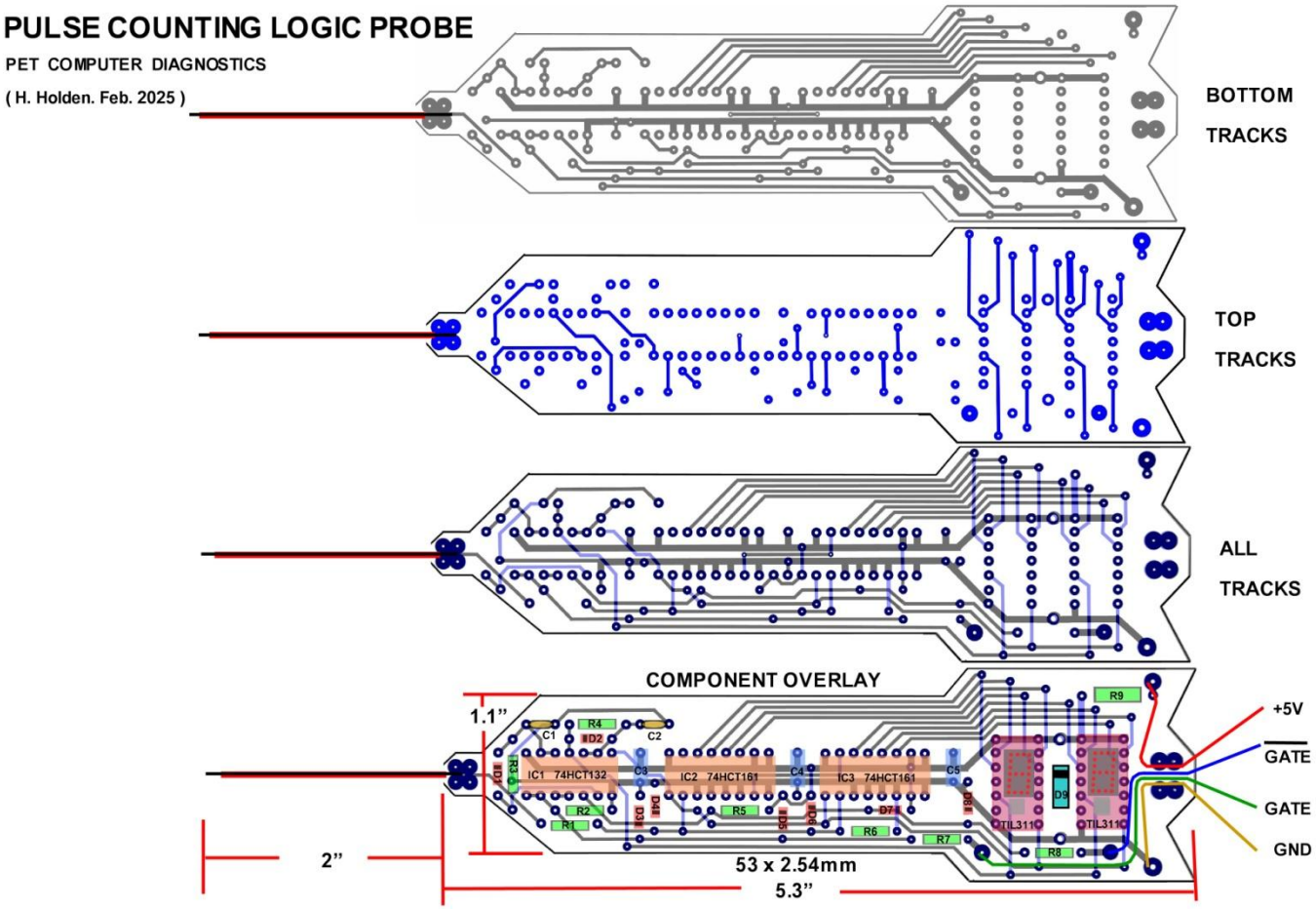
For a simple gated logic probe to work requires that in the gated time, it counts pulses in that window. At the end of the count, the data is latched in the displays, then shortly after that with a small delay the counter IC's are cleared. The display is blanked during counting time, so that the visible display appears clean and stable.

A Hex display is handy because then the count can range from 0 to 255 with two counter IC's and with two Display Modules presented as a Hex value from 00 to FF, and that "byte" can be readily converted into a Decimal value. Decimal counter IC's such as the 74HCT160 could be used, but that doesn't make best use of the Hex displays and limits the count to 99, unless another counter IC and display module is added.

It is useful to have a small delay at the end of a gating window (in his case in the order of 500nS) as could be seen from the previous timing diagrams, this can help count pulses, for example leading to the generation of the 4th NEXT pulse in the PET.



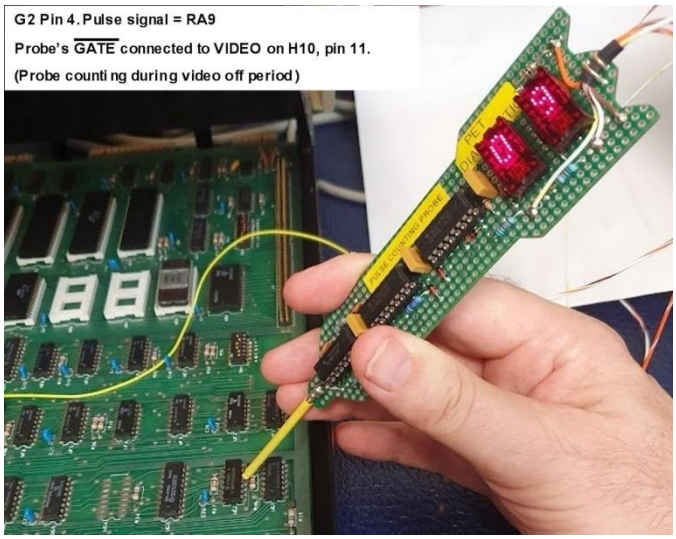
Since the probe could be misused by accidentally powering it in reverse or by applying excessive voltages, some protections are provided. If excessive power supply voltage is applied (say connecting it to 12V by mistake) or applied reverse polarity the power Zener diode conducts in both cases, there is a sacrificial 1/8 watt 1 Ohm resistor that will vaporise and behave as a fuse. It pays to mount that a little clear of the pcb. It drops only around 100mV to 150 mV depending on the display brightness.

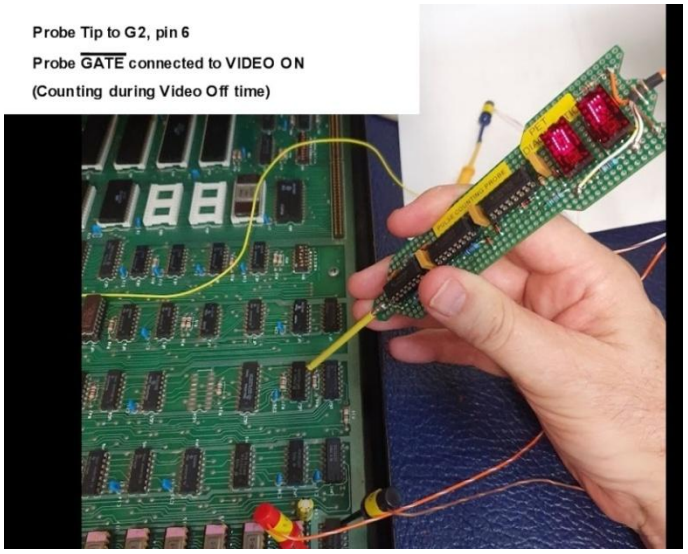


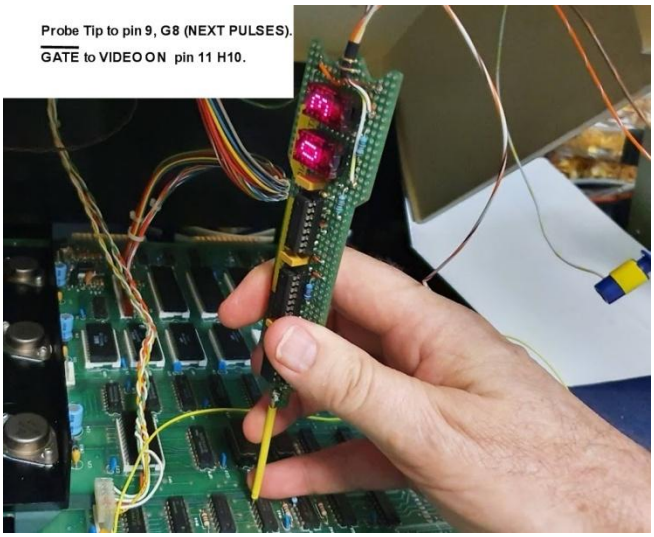
The diodes D1 and D2 and the resistors R3 and R4 allow selective delays of leading or trailing pulse edges. The is because the outputs of the 74HCT132 gates have a low resistance and can charge or discharge the small added capacitances quickly via the diodes, but the charge or discharge pathway, as selected, can be slowed down with the resistors to create specific delays. In this case a 500nS and a 150nS delay was used to allow the counter to pick up (count) a pulse on the end of the GATE time and also to latch the count shortly before the counters were cleared for the next pulse counting cycle.

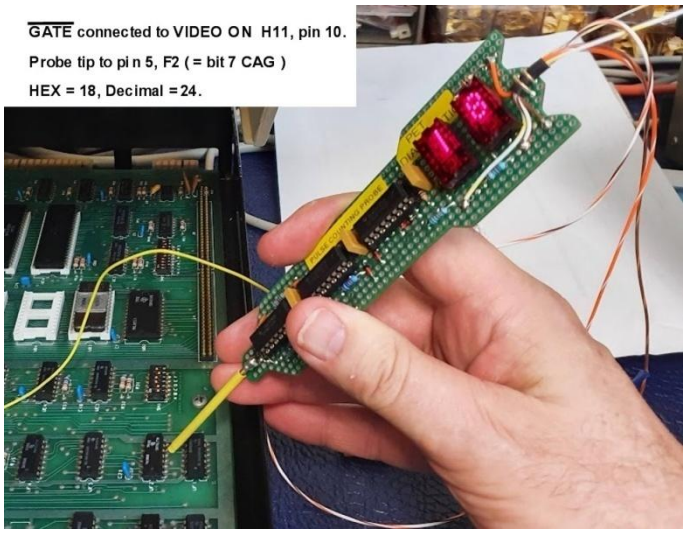
The probe has two optional inputs/GATE and GATE, depending on the polarity of the pulses available to use as the gate pulse. For example, to count pulses at the probe tip, when the VIDEO ON signal is LOW, the /GATE input would be used. Or to count pulses while the gating signal is high, the GATE input would be used.

The images below show some verification tests using the Pulse Counting Probe:









When the probe is gated to count during the VIDEO OFF time, it will count 3 of the 4 NEXT pulses, as noted, this is because the 1st NEXT pulse precedes the VIDEO OFF time a sit occurs just before the trailing end of the VIDEO ON time.

The probe for example can have its GATE input connect to HORZ DISP ON pulse and actively count /RA1 pulses for a time of just over 40uS (where it counts 20 pulses and the HEX Display reads 14) and then it displays them for close to 24uS of the 64uS total time, or about 37.5% of the time and the display is still is very bright. Even with a 5 to 10% duty cycle for the display ON time, the LED's in these modules are easy to see.

****